Elektronika analogowa i cyfrowa

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Z menu "File" wybierz "New Project"

Select "File" then "New Project"



Należy wpisać dowolną nazwę projektu. Jako "Top-level source type" należy wybrać "HDL"

Any project name must be typed. "Top-level source type" must be "HDL"

	New Project Wizard	
Create New Project Specify project locati	on and type.	
Enter a name, locat	ions, and comment for the project	
N <u>a</u> me:	Firststep	
Location:	/home/mtanas/ISE/Firststep	<u></u>
Working Directory:	/home/mtanas/ISE/Firststep	<u></u>
Description:		
Select the type of to	op-level source for the project	
Top-level source ty	pe:	
HDL		\$
More Info		Next > Cancel

Parametry projektu i urządzenia proszę wybrać dokładnie takie jak na screenshocie.

The project and device parameters must be exactly like ones on the screenshot New Project Wizard

Project Settings

Specify device and project properties.

Select the device and design flow for the project

Property Name	Value	
Evaluation Development Board	None Specified	\$
Product Category	All	\$
Family	Spartan3E	\$
Device	XC3S100E	\$
Package	VQ100	\$
Speed	-5	\$
The Louis Course Tree		
Iop-Level Source Type	HDL	
Synthesis Tool	XST (VHDL/Verilog)	\$
Simulator	ISim (VHDL/Verilog)	\$
Preferred Language	VHDL	\$
Property Specification in Project File	Store all values	\$
Manual Compile Order		
VHDL Source Analysis Standard	VHDL-93	\$
Enable Message Filtering		

Pokaże się podsumowanie parametrów projektu. Należy kliknąć "Finish"

The project summary will be presented. Click "Finish"

New Project Wizard					
Project Summary Project Navigator will create a new project with the following specifications.					
Project: Project Name: Firststep Project Path: /home/mtanas/ISE/Firststep Working Directory: /home/mtanas/ISE/Firststep Description: Top Level Source Type: HDL Device: Device: xc3s100e Package: vq100 Speed: -5 Top-Level Source Type: HDL Synthesis Tool: XST (VHDL/Verilog) Simulator: ISim (VHDL/Verilog) Preferred Language: VHDL Property Specification in Project File: Store all values Manual Compile Order: false VHDL Source Analysis Standard: VHDL-93 Message Filtering: disabled					
More Info Cancel					

Z menu "Project" wybierz "New source"

Click "Project" then "New source"



Jako "Source type" wybierz "VHDL Module" Nazwę pliku wpisz dowolną.

"Source type" must be "VHDL module". As "File name" type anything.

New Sour	rce Wizard
Select Source Type Select source type, file name and its location	on.
 IP (CORE Generator & Architecture Wizar Schematic User Document Verilog Module Verilog Test Fixture VHDL Module 	<u>F</u> ile name:
 WHDL Library VHDL Package VHDL Test Bench Embedded Processor 	firstchip Lo <u>c</u> ation: /home/mtanas/ISE/Firststep
	✓ <u>A</u> dd to project
More Info	<u>N</u> ext > Cancel

Nazwę układu ("Entity name") wpisz dowolną. Porty we/wy ustaw jak na screenshocie.

As "Entity name" type anything. I/O ports must be set as in the screenshot

	New Sou	irce Wizard				
Define Module Specify ports for n	nodule.					
Entity name	firstchip					
Architecture name	Behavioral					
Po	rt Name	Direction	Bus	MSB	LSB	•
Input		in 🗘				
Output		out 🗘				
		in 🖨				=
		in 🗘				
		in 🗘				
		in 🗘				
		in 🗘				
		in 🗘	Ì			-
More Info		< <u>B</u> a	ick	<u>N</u> ext >	Cance	

Gdy pojawi się "Summary" kliknij "Finish"

When the "Summary" appears click "Finish"

_			New Source Wizard	
Su	mmary Project Navigator wil	ll create a ne	ew skeleton source with the following specifications	
4 0 0 0	Add to Project: Yes Gource Directory: /ho Gource Type: VHDL M Gource Name: firstchi	me/mtanas/l odule ip.vhd	SE/Firststep	
E /	Entity name: firstchip Architecture name: B Port Definitions:	ehavioral	in	
	Output	Pin	out	
<u>N</u>	<u>1</u> ore Info		< <u>B</u> ack <u>Finish</u> Cano	el

ISE wygeneruje szkielet kodu VHDL naszego układu.

The core of VHDL code of our chip will be generated by ISE



File Edit View Project Source Process Tools Window Layout Help

Rozwiń listę "Synthetize – XST" i kliknij prawym klawiszem na "Check syntax". Wybierz "Run".

Expand the list "Synthetize – XST", right click on "Check syntax" and click "Run".

File Edit View Project Source Proce	ess Tools W	/indow Layout Help	
	lic) »	* * 8 8 * 8 🔊 🗟 🗆 • * *	🕨 🗴 🗶 💡
esign OD	75		
* View® 郁 Implementat 〇 國 Simulat	13	Dependencies:	
	14	Deviaion	
Hierarchy	15	Revision:	
Hirststep	10	Revision 0.01 - File Cleated	
XC3S100e-SVq100	1/	Additional comments:	
	- 18		
•••	= 19	library IPPP.	
	120	use IFFF STD LOCIC 1164 ML.	
	- 21	use TERE.STD_DOGIC_TI04.ADD,	
	1 22	Uncommont the following library dec	laration if using
x	23	orithmetic functions with Signed or	Ungigned values
	24	allemmetre functions with signed of	Unsigned values
-	25	use IEEE.NOMERIC_SID.ADD;	
	20	Uncomment the following library dec	laration if instantiat
	20	any Viling primitives in this code	Taración il instantiat
	20	alibrary UNISTM.	
	29	IDIALY UNISIM,	
No Processes Running	30	- use owisim. vcomponents.all;	
Processes: firstchin - Behavioral	31	optitu firstship is	
Processes: Instellip - Denavioral	32	Part / Trant in amp Logic	
Design Summary/Reports	33	Port (Input : In SID_BOGIC;	
User Constraints	34	output : out SID_LOGIC);	
Synthesize - XST	35	end lirstenip;	
View RTL Schematic	36	anabitastuna Dabawianal of finatabin i	20 C
View Technology Sche	37	architecture Benavioral of firstchip 1	.5
💫 Check	3.8		
Gener L Pun		begin	
E Impleme ReRun			
Generate Rerun All		and Debautanal	
		end Benavioral;	
View Text Report		Decign Summany	× 🖻
Start Design View lext Report		Design Summary	
onsole <u>Force Process Up</u>	o-to-Date		
NFO:ProjectMgmt > Implement Top N	1odule	completed successfully.	
Launching Design	Stratogias		
Started : "Laund	suategies	firstchin vhd"	
Process Properti	es		
		1	
	~~~~~~		

ISE powinien potwierdzić poprawności składni.

ISE shall confirm corectness of the syntax.

E E	le <u>E</u> dit <u>V</u> iew P <u>r</u> oject <u>S</u> ource <u>P</u> roc	ess <u>1</u>	<u>T</u> ools <u>W</u> in	dow La <u>v</u> out <u>H</u> elp
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E.	Hierarchy	-	15	Revision:
	🗏 🧧 Firststep	$\equiv$	16	Revision 0.01 - File Created
6	☐ ☐ xc3s100e-5vq100	10	17	Additional Comments:
	🔤 🔚 🛗 firstchip - Behavioral (firs	=	18	
00		Ξ	19	
a		10	20	library IEEE;
e			21	use IEEE.STD_LOGIC_1164.ALL;
0		4	22	
			23	Uncomment the following library declaration if using
2		%	24	arithmetic functions with Signed or Unsigned values
		126	25	use IEEE.NUMERIC_STD.ALL;
			26	The second the full scient library dealerships if instantistics
		26	27	Uncomment the following library declaration if instantiating
			28	any Allinx primitives in this code.
		9	29	use UNISIM,
	No Processes Running	$\bigcirc$	21	use onisim.vcomponents.all,
BH	Processes: firstchip - Behavioral	-	32	entity firstchip is
14	Design Summary/Beports		32	Port (Input : in STD LOGIC:
20	<ul> <li>Design Utilities</li> </ul>		34	Output : out STD LOGIC):
	🕀 🈼 User Constraints		35	end firstchip;
91	🖻 🚺 _ Synthesize - XST		36	
_	View RTL Schematic		37	architecture Behavioral of firstchip is
	View Technology Sche		38	*
	Generate Post-Synthe		39	begin
	The Design		40	
	Generate Programming File		41	
	🗉 🛞 Configure Target Device		42	end Behavioral;
	Analyze Design Using Ch	(	•	
>	Start 📑 Design 🖺 Files 🚺 🕨	Σ		Design Summary 🗙 📄
Con	sole			
С	ompiling vhdl file "/home/mtana	s/ISE	/Firstst	ep/firstchip.vhd" in Library work.
A	rchitecture behavioral of Entit	y fir	stchip i	s up to date.
Р	rocess "Check Syntax" completed	suco	essfully	
•				
	Console 😰 Errors 🔬 Warnings	K F	ind in Files	Results
Sav	e the active file			

Zmień "View" z "Implementation" na "Simulation"

Change the "View" from "Implementation" to "Simulation"



Kliknij prawym klawiszem na kod układu i wybierz "New source"

Right click on the device's code and select "New source"



Jako "Source type" wybierz "VHDL Test Bench" Nazwę pliku wpisz dowolną

"Source type" must be "VHDL Test Bench". As file name type anything.

New Sour	rce Wizard
Select Source Type Select source type, file name and its location	on.
BMM File         ChipScope Definition and Connection File         Implementation Constraints File         IP (CORE Generator & Architecture Wizar         MEM File         Schematic         User Document         Verilog Module         Verilog Test Fixture         VHDL Module         VHDL Library         VHDL Test Bench         Embedded Processor	File name: firstchiptestbench Location: /home/mtanas/ISE/Firststep
More Info	<u>N</u> ext > Cancel

Jako "Associate Source" wybierz plik z kodem "VHDL Module" (patrz slajd 7).

As "Associate Source" select the "VHDL Module" file (see slide 7)

New Source	e Wizard
Associate Source Select a source with which to associate the	new source.
firstchip	
More Info	< <u>B</u> ack <u>N</u> ext > Cancel

## Gdy pojawi się "Summary" kliknij "Finish"

When "Summary" appears click "Finish"

immary	
Project Navigator will create a new skeleton sourc	ce with the following specifications.
Add to Project: Yes Source Directory: /home/mtanas/ISE/Firststep Source Type: VHDL Test Bench Source Name: firstchiptestbench.vhd Association: firstchip	

Rozwiń listę "ISim Simulator", kliknij prawym klawiszem na "Behavioral check syntax" i kliknij "Run"

Expand list "Isim Simulator", right click on "Behavioral check syntax" and click "Run"

)es	ign 🕀 🗆 🖉 🗶			
Ŧ	View 🔿 🄯 Implementat 💿 🧱 Simulat	34	ENTITY firstchiptestbench IS	
	Behavioral 🗘	3	END firstchiptestbench;	
h	Hierarchy	3	ADQUITEDOTUDE behavior OF firstshiptastharsh IC	
	- 🔄 Firststep	12 31 21	ARCHITECTORE Denavior of firstchiptestbench is	
	xc3s100e-5vq100 firstchiptestbench - behavid	= 4	Component Declaration for the Unit Under Test (UUT)	
	🐂 uut - firstchip - Behavior	4		
		= 4:	COMPONENT firstchip	
71		4	PORT (	
		44	Input : IN std_logic;	
2		% 4	Output : OUT sta_logic	
		%	END COMPONENT:	
-		× 4		
		- 4		
		G 51	Inputs	
	No Processes Running	5	<pre>signal Input : std_logic := '0';</pre>	
	Processo fortabista thank haber	52		
Ŧ,	- M USim Simulator	5.	Outputs	
1	Behavioral Check Syn	54	No clocks detected in port list. Replace (clock) below with	
	Simulate Behavioral	5	appropriate port name	
1		5		
_		51	<pre>constant <clock>_period : time := 10 ns;</clock></pre>	
ш		5.		
		61	BEGIN	
		6		
		63	Instantiate the Unit Under Test (UUT)	
		6.	uut: firstchip PORT MAP (	

Ooops. Coś poszło nie tak.

Ooops. Something wrong.

ISE Project Navigator (P.20131013) - /home/mtanas/ISE/Firststep/Firststep.xise - [firstchiptestbench.vhd] File Edit View Project Source Process Tools Window Layout Help n » 🏓 🔑 😥 🏓 🗟 💫 🕾 🗄 🗖 🖻 🥬 🖗 🕨 🗴 📌 💡 🗋 🆻 🗟 🧖 🖕 👗 🗅 🗅 🗙 🗎 Design 00X • 41 View 🔿 🔯 Implementat 💿 🌆 Simulat COMPONENT firstchip 42 Behavioral ¢ PORT ( 43 Input : IN std_logic; 44 Hierarchy 8 Output : OUT std_logic 45 🔄 Firststep 5 ); 46 xc3s100e-5vq100 😑 🔝 firstchiptestbend 47 END COMPONENT; 😼 uut - firstchip - Behavior 48 49 50 --Inputs ٨ signal Input : std_logic := '0'; 51 . 52 % 53 --Outputs % signal Output : std_logic; 54 -- No clocks detected in port list. Replace <clock> below with ** 55 -- appropriate port name 56 0 57 constant <clock>_period : time := 10 ns; 58 Run Failed: Check Syntax 65 59 Processes: firstchiptestbench - beha 60 BEGIN 🗄 🎾 🛛 ISim Simulator 61 -- Instantiate the Unit Under Test (UUT) 62 Simulate Behavioral . uut: firstchip PORT MAP ( 63 91 Input => Input, 64 Output => Output 65 ); 66 67 68 -- Clock process definitions 69 <clock>_process :process 70 begin × 🗎 × 🗎 🍃 Start 🛤 Design 🖺 Files 🚺 🖡 📡 Design Summary firstchip.vhd firstchiptestbench.vhd Console Determining compilation order of HDL files HDLCompiler:488 - "/home/mtanas/ISE/Firststep/firstchiptestbench.vhd" Line 58: Illegal identifier : _period 0 :HDLCompiler:488 - "/home/mtanas/ISE/Firststep/firstchiptestbench.vhd" Line 69: Illegal identifier : process 0 :HDLCompiler:488 - "/home/mtanas/ISE/Firststep/firstchiptestbench.vhd" Line 72: Illegal identifier : _period • :HDLCompiler:488 - "/home/mtanas/ISE/Firststep/firstchiptestbench.vhd" Line 74: Illegal identifier : _period 0 " Line 04. Tllegel identifier UDI Compilari 400 📃 Console 🙆 Errors 🔔 Warnings 🙀 Find in Files Results

Znajdź **wszystkie** wystąpienia "<clock>" i zamień je na "clock" (usuń nawiasy).

Find **every** "<clock>" and replace it with "clock" (remove braces)



Dopisz linię "signal clock : std_logic;" zaraz przed "BEGIN"

Type line "signal clock : std_logic;" just before "BEGIN"

57	
58	<pre>constant clock_period : time := 10 ns;</pre>
59	
60	<pre>signal clock : std_logic;</pre>
61	
62	BEGIN
63	

Ponownie uruchom "Behavioral check syntax" Teraz powinno być wszystko w porządku.

Rerun "Behavioral check syntax".

Now everything shall be OK

ø				ISE Project Navigator (P.20131013) - /home/mtanas/ISE/Firststep/Firs	tste
Ē	ile <u>E</u> dit <u>V</u> iew P <u>r</u> oject <u>S</u> ource <u>P</u> roc	ess	<u>T</u> ools <u>W</u> in	dow Layout <u>H</u> elp	
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¥	View 🔿 🎒 Implementat 🖲 🎆 Simulat		46	END COMPONENT:	
_	Behavioral 🗘		48		
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í1	ineratory Stretsten		50	Inputs	
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a	🖫 🖫 uut - firstchip - Behavior	10	53	Outputs	
			54	<pre>signal Output : std_logic;</pre>	
		A	55	- No clocks detected in port list. Replace <clock> below with</clock>	
_		~	56	appropriate port name	
•		%	57	constant class period , time or 10 per	
-		%	58	constant clock_period : time := 10 hs;	
		XA	59	signal clock : std logic:	
		70	61	bighar brook , bad_rogio,	
		0	62	BEGIN	
	No Processos Rupping		63		
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Pr	Processes: firstchiptestbench - behav		65	uut: firstchip PORT MAP (	
	🖻 🎾 🛛 ISim Simulator		66	Input => Input,	
μ5,	🔃 😡 Behavioral Check Syn		67	Output => Output	
Dirt.	Simulate Behavioral		68	);	
1			69		
-			70	Clock process definitions	
			71	clock_process :process	
			72	begin	
			73	clock <= '0';	
			74	wait for clock_period/2;	
			75	clock <= 'l';	
5	Start In Design in Files	X		Design Summary X 🖹 firstchin yhd X	× F
-	i Design				
Con	sole				
F	arsing VHDL file "/home/mtanas/ arsing VHDL file "/home/mtanas/	'ISE/ /ISE/	Firststep Firststep	/fırstchip.vhd" into library isim_temp /firstchiptestbench.vhd" into librarv isim temp	
F	rocess "Behavioral Check Syntax	(" CO	mpleted s	uccessfully	
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	Console 🙆 Errors 🔬 Warnings	8	Find in Files	Results	

#### Plik Maszyna Widok Wejście Urządzenia Pomoc ISE Project Navigator (P.20131013) - /home/mtanas/ISE/Firststep/Firststep. 📄 File Edit View Project Source Process Tools Window Layout Help Σ 📌 💡 🗋 🆻 🖟 888 G., E. AXDBX ls) » 🌶 **k?** Design 00X 46 ); View 🔿 🔯 Implementat 💿 🎆 Simulat END COMPONENT; 47 Behavioral \$ 48 49 Hierarchy 50 --Inputs 🔄 Firststep signal Input : std_logic := '0'; 51 xc3s100e-5vq100 52 --Outputs 53 🐘 uut - firstchip - Behavior signal Output : std_logic; 54 -- No clocks detected in port list. Replace <clock> below with 55 A 56 -- appropriate port name 57 % constant clock_period : time := 10 ns; 58 % 59 signal clock : std_logic; 60 * 61 Þ 62 BEGIN 63 No Processes Running ► -- Instantiate the Unit Under Test (UUT) 64 Processes: firstchiptestbench - behav uut: firstchip PORT MAP ( 65 70 ė. 🎾 ISim Simulator 66 Input => Input, Nehavioral Check Syn... Output => Output 67 ); 70 Rerun All -- Clock process definitions clock_process :process Stop begin clock <= '0'; wait for clock_period/2; Process Properties.. clock <= '1'; 🍃 Start 🔍 Design 🖺 Files 🚺 🕨 🗵 Design Summary X firstchip.vhd × Console Parsing VHDL file "/home/mtanas/ISE/Firststep/firstchip.vhd" into library isim_temp Parsing VHDL file "/home/mtanas/ISE/Firststep/firstchiptestbench.vhd" into library isim_temp Process "Behavioral Check Syntax" completed successfully Console 🙆 Errors 🔬 Warnings 🙀 Find in Files Results Run highlighted process

Uruchom "Simulate behavioral"

Run "Simulate behavioral"

ISE wyświetli przebieg sygnałów na nóżkach układu.

Linie są płaskie bo nasz układ na razie nic nie robi.

ISE will show the signal waveform on the device's pins.

Lines are flat because our device does nothing so far.

